



VIT

Vellore Institute of Technology  
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING

Continuous Assessment Test - I, August 2018

B.Tech, Fall Semester 2018-19

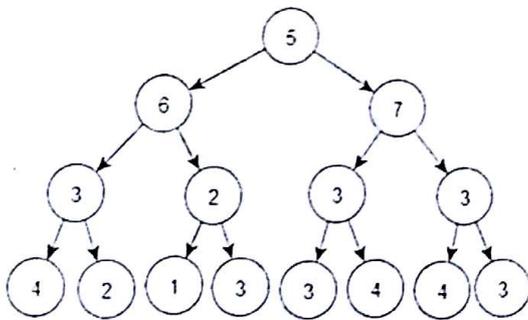
Course Code	: CSE4001	Duration	: 90 Minutes.
Course Name	: Parallel and Distributed Computing	Max. Marks	: 50
School	: SCOPE	Slot	: B2

Answer All the Questions

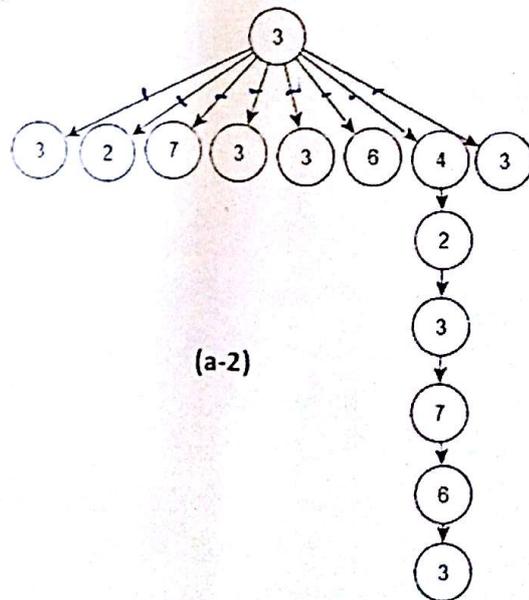
(5\*10=50 Marks)

1. (a) For the given weighted task-dependency graphs, determine the following for each graph: [6]

- (i) Maximum degree of concurrency
- (ii) Critical path length
- (iii) Average degree of concurrency



(a-1)



(a-2)

(b) Explain the task dependency graph and its significance in parallel algorithm design with an appropriate example. [4]

2. Construct a diagram for 16x16 omega switching network. Observe its network interconnection to give explanation for: (10)

- (i) type of network (i.e. static/dynamic, direct/indirect, etc.)
- (ii) the routing
- (iii) blocking/nonblocking properties
- (iv) the interstage connection scheme
- (v) the number of stages
- (vi) the number of switches, the last two of which must be in relation to the number of nodes.
- (vii) trace the path for routing the data from the node 0010 to 1010.

3. (a) Illustrate the State transition diagram of a three State Cache Coherence Protocol. (3)



(b) Construct the state table for write invalidate protocol (Cache Coherence) for the following instruction. The Seq.No represents the Sequence no in which instructions are executed. Variables X=2 is stored in Processor 0 and Global Memory, Y=9 is stored in Global Memory and Z=6 is stored in Processor 1 and Global Memory. (7)

Seq. No	Instruction at Processor 0	Instruction at Processor 1
1	$X = X + 1$	$Y = Y + Z$
2	$X = X + Y$	$Z = Z + 2$
3	$Y = X + Y + Z$	
4		$X = X + Y + Z$
5	$Z = X + Y + Z$	
6	$X = X + 1$	$Y = Y + 1$

4. Describe the architecture of an Ideal Parallel Computer (PRAM) and give the comparison of SIMD and MIMD architectures. (10)

5. (a) Explain the differences between Scalar and Vector processors. (4)

(b) Explain how the computational complexity can be reduced using 'Vector Processing' technique with suitable example. (6)